REMARKS

Claims 1-20 remain pending in the application. Claim 1 has been amended.

35 U.S.C. § 102 Rejection:

Claims 1-5 were rejected under 35 U.S.C. § 102(b) as being anticipated by Clauburg, U.S. Patent 6,389,018. Applicant respectfully traverses this rejection.

The cited reference does not teach or suggest all of the elements of independent claim 1. Clauberg teaches an apparatus is provided for processing a sequential stream of fixed length cells received via a slotted data transmission medium. The cells may be asynchronous transfer mode (ATM) cells. The apparatus utilizes a demultiplexer to create N (N=2,3,4 . . .) sub-streams of cells from the input stream and to pass each sub-stream to one of N processing paths. Each of the processing paths is identical and they operate in parallel. The cell sub-streams are fed into the processing paths in a chronological, staggered manner where the time between one sub-stream being fed into its processing path and the next sub-stream being fed into another processing path is equal to the slot duration of the transmission medium. Finally, the apparatus utilizes a multiplexer to combine the processed sub-streams into an output stream which maintains both the sequential order of the cells and their arrangement in the slots of the slotted transmission medium.

Applicant's independent claim 1 recites, in pertinent part:

"A digital system that comprises: a plurality of units operating at a first clock rate, each unit configured to independently process a sequence of data items; and a domain crossover element configured to receive a stream of data items at a second clock rate different from the first clock rate and configured to distribute separate sequences of data items through separate ports to the plurality of units" (emphasis added).

Clauberg does not teach or suggest this combination of features. In particular, Clauberg does not teach or suggest a plurality of units operating at a first clock rate and a domain crossover element configured to receive a stream of data items at a second clock rate. In the office action, the Examiner contends that Clauberg teaches a plurality of units operating at a first clock rate (Fig. 3C, 14.1-15.1, 14.2-15.2, etc.) and a domain crossover element (Fig. 3C, demux 12) configured to receive a stream of data items at a second clock rate (for every 't', col. 3, lines 43-56). Furthermore, in rejecting claim 2, the Examiner contends that Clauberg teaches that the second clock rate is greater than the first clock rate, citing Clauberg at col. 3, lines 43-45, and further contends that the rate of every 't'> rate of 't0+xT'. Applicant respectfully disagrees with the Examiner's characterization, and submits that that Clauberg provides no teaching or suggestion that demultiplexer 12 shown in Fig.'s 3A-3G of receives a data stream at a clock rate different from the clock rate at which the processing units operate.

In col. 3, lines 43-56, Clauberg states:

> "In FIG. 2, a typical stream 30 of fixed length cells A-G is illustrated. The slotted character of the transmission medium is indicated by dividing up the time axis into slots. The slot duration is denoted by the letter `T`. The snapshot shown in FIG. 2 is taken at the time t=t.sub.0. The stream 30 of fixed length cells A-G will now be fed through the inventive parallel processing unit 9 illustrated in FIG. 1. Snapshots are taken at the times t=t.sub.0 +T, t=t.sub.0 +2T, t=t.sub.0 +3T, t=t.sub.0 +4T, t=t.sub.0 +5T, t=t.sub.0 +6T, and t=t.sub.0 +7T. This sequence of snapshots are illustrated in FIGS. 3A-3G. As can be seen from this sequence, the first sub-stream of cells (note that in the present example a sub-stream of cells consists of one cell only) is fed into the first processing path 13.1, the second sub-stream is fed into the second path 13.2 one slot duration later, and so forth." (emphasis added).

Applicant can find no teaching or suggestion of different clock rates in this citation, and respectfully submits that the Examiner's characterization that the rate of every 't'> rate of

't0+xT' is erroneous. In the above citation, the designation 'T' is indicative of one slot duration, not of a clock rate. The snapshot taken in Fig. 2 is taken at time t=t.sub.0, indicating that no time has elapsed at the time of the snapshot. The time t=t.sub.0 +T indicates that one slot duration has elapsed, the time t=t.sub.0 +2T indicates that two slot durations have elapsed, and so forth, but does not indicate differing clock rates, nor do these times indicate that 't'> rate of 't0+xT' as alleged by the Examiner. Applicant further notes that in each of the examples given in the citation above, **t = t0+xT**, contrary to the Examiner's assertion that 't' > rate of 't0+xT'.

The Examiner's attention is directed to Fig.'s 3A-3G of Clauberg, which are described therein as follows: "FIGS. 3A-3G are schematic snapshots of a parallel processing unit with N=5 parallel processing paths used to illustrate the routing and processing of cells." In Fig. 3A, after one slot duration ($t=t_0+T$), cell A is input into demultiplexer 12. In Fig. 3B, after two slot durations ($t=t_0+2T$), cell A is input into processing unit 14.1, while cell B is input into demultiplexer 12. In Fig. 3C, after three slot durations ($t=t_0+3T$), cell A is forwarded to processing unit 15.1, cell B is input into processing unit 14.2, and cell C is input into demultiplexer 12. In Fig. 3D, after four slot durations (($t=t_0+4T$), cell A is output from processing unit 15.1 into multiplexer 19, cell B is forwarded to processing unit 15.2, cell C is input into processing unit 14.3, and cell D is input into demultiplexer 12. In other words, the rate at which cells progress through the processing units is the **same rate** at which cells are received by demultiplexer 12, and thus the clock rates at which they operate are the same. Thus, even if processing units are not processing a cell during a given slot duration, they nevertheless process a received cell at the same rate at which cells are received by multiplexer 12. Accordingly, Applicant submits that Clauberg does not teach or suggest "a plurality of units operating at a first clock rate, each unit configured to independently process a sequence of data items; and a domain crossover element configured to receive a stream of data items at a second clock rate **different** from the first clock rate" as recited in independent claim 1.

For at least the reasons stated above, Applicant submits that Clauberg does not teach or suggest all of the elements of claim 1, and thus respectfully requests removal of the 35 U.S.C. § 102(b) rejection.

35 U.S.C. § 103 Rejections:

Claims 6-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Clauberg in view of Chung, U.S. Patent 5,764,895. Claim 10 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Clauberg in view of Chung and in further view of a 5-Stage Johnson Counter ('Johnson Counter'), Talarek, U.S. Patent 6,628,679, and Segal, U.S. Patent 4,685,101. Claims 17-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Clauberg in view of Talarek and Segal. Claim 20 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Clauberg in view of Talarek and Segal and in further view of Kariquist, U.S. Patent Application Publication 2003/0063626. Applicant respectfully traverses these rejections.

The cited references, taken singly or in combination, do not teach or suggest all of the elements of the independent claims. With regard to claims 6-10, Applicant notes these claims are dependent upon claim 1 and thus incorporate its limitations. Thus, for at least the reasons stated above with regard to the § 102 rejection of claim 1, Applicant submits that the cited references, taken singly or in combination, do not teach or suggest "a plurality of units operating at a first clock rate, each unit configured to independently process a sequence of data items; and a domain crossover element configured to receive a stream of data items at a second clock rate different from the first clock rate" as recited in claim 1.

With respect to claim 17 and it associated dependent claims, Applicant submits that for reasons similar to those stated above with regard to the § 102 rejection, the cited references taken singly or in combination do not teach or suggest "A method of distributing a stream of data items received at a first clock rate among a plurality of processing units operating at a second, **slower** clock rate" as recited in claim 17. In the office action, the Examiner contends that Clauberg describes a demultiplexer distributing

a stream of data items received at a first clock rate among a plurality of processing units operating at a second, slower clock rate. However, as discussed above in regard to the § 102 rejection, cells progress through the processing units at the same rate at which cells are received by demultiplexer 12, and thus the processing units and demultiplexer 12 of Clauberg are operating at the same clock rate.

For at least these reasons, Applicant submits that a case of obviousness has not been established with regard to the § 103(a) rejections, and thus their removal is respectfully requested.

Allowed Claims:

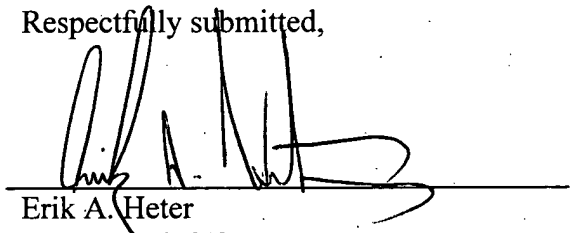
Claims 11-16 were allowed. Applicant appreciates Examiner's consideration of these claims.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-74100/BNK.

Respectfully submitted,



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